

FIG. 1a is a block diagram of a communication system. The system includes an Arithmetic Encoder (1) which receives input s_n and outputs x_k to a Channel (2). The Channel (2) outputs r_k to a Sequential Decoder (3). The Sequential Decoder (3) outputs \hat{x}_k to an Arithmetic Decoder (4). The Arithmetic Decoder (4) outputs \hat{s}_n . The Sequential Decoder (3) and Arithmetic Decoder (4) are connected by a feedback loop. The Sequential Decoder (3) also receives "Coder Header Info" from the Arithmetic Encoder (1). The Arithmetic Decoder (4) also receives "Coder Header Info" from the Sequential Decoder (3).

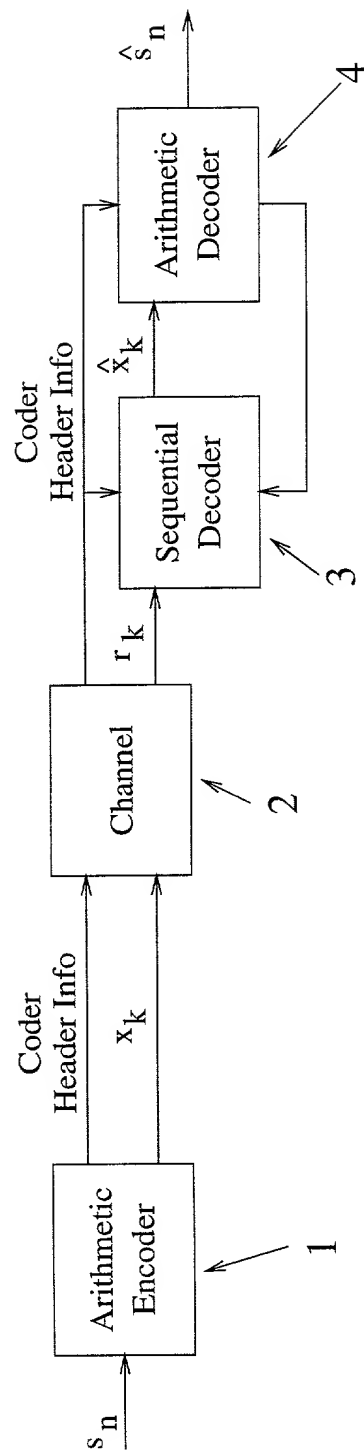


FIG. 1 a

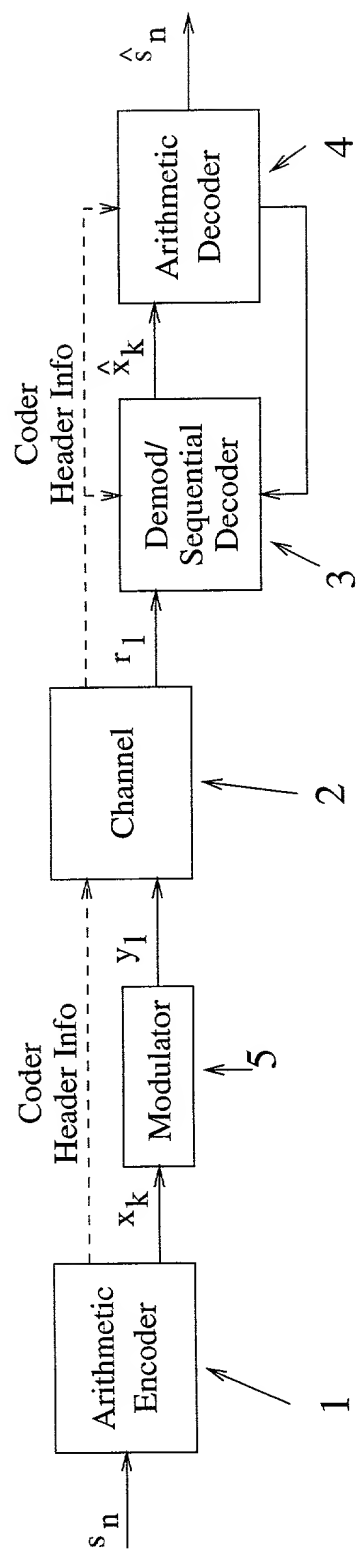


FIG. 1b

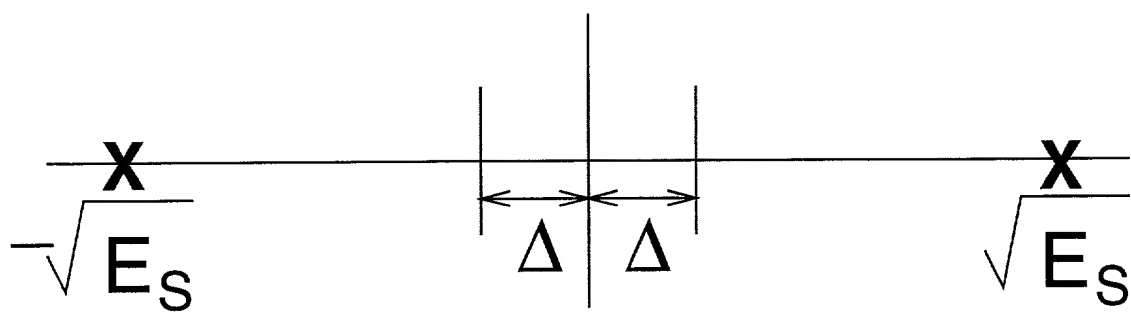


FIG. 2

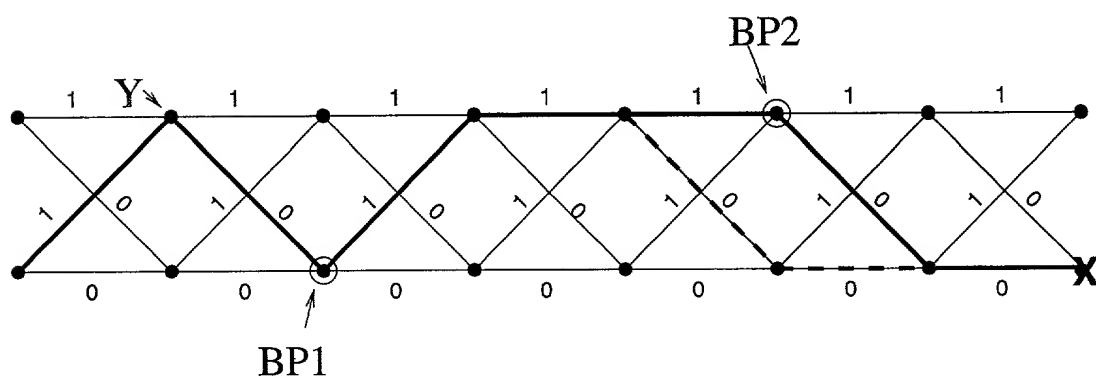


FIG. 3

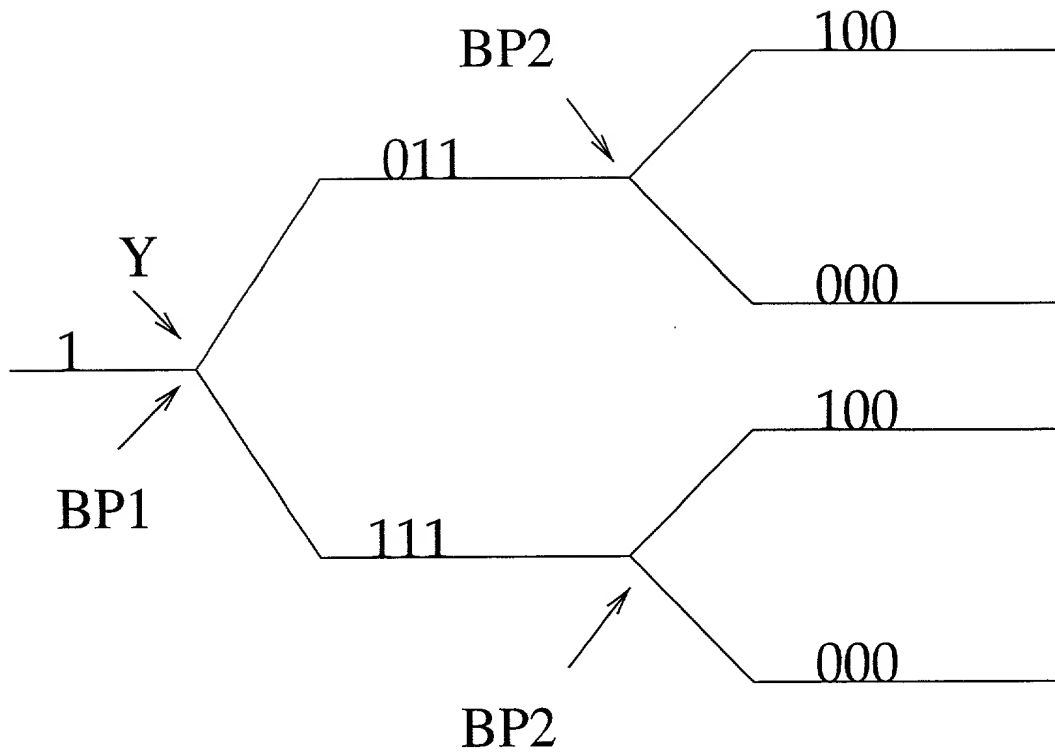


FIG. 4

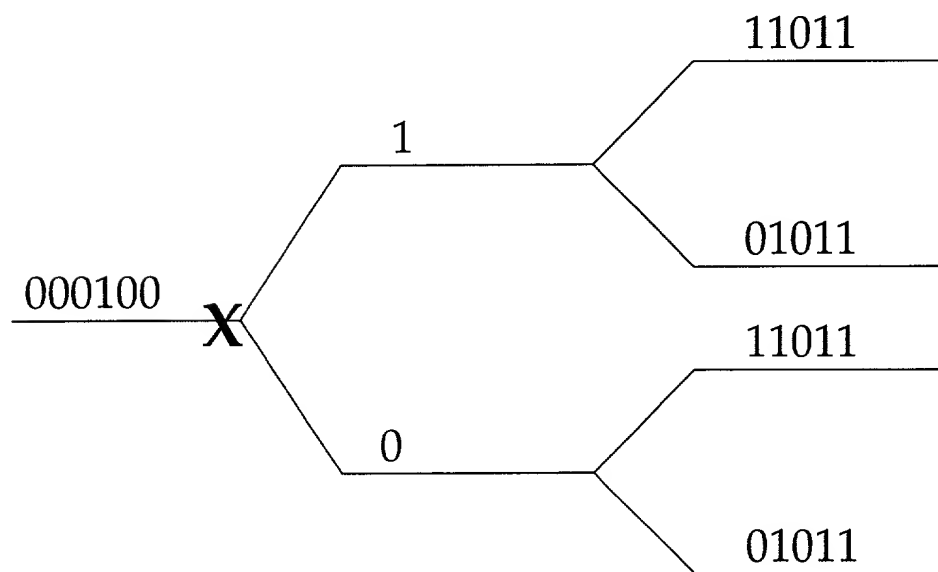


FIG. 5

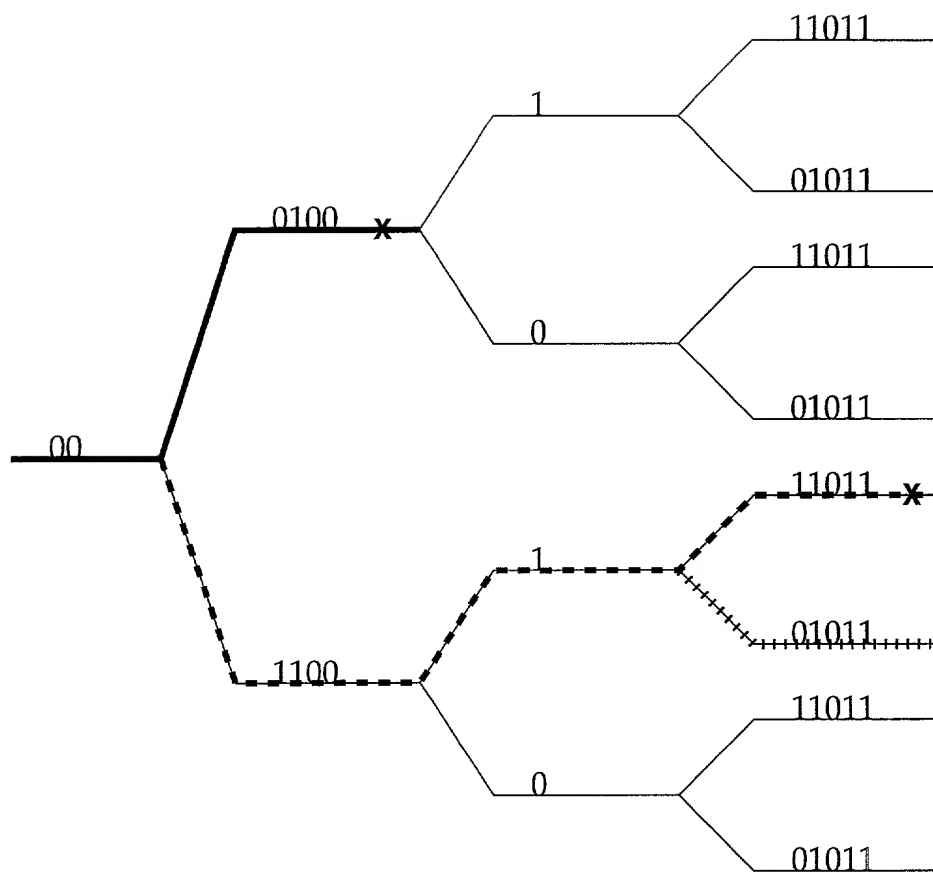


FIG. 6

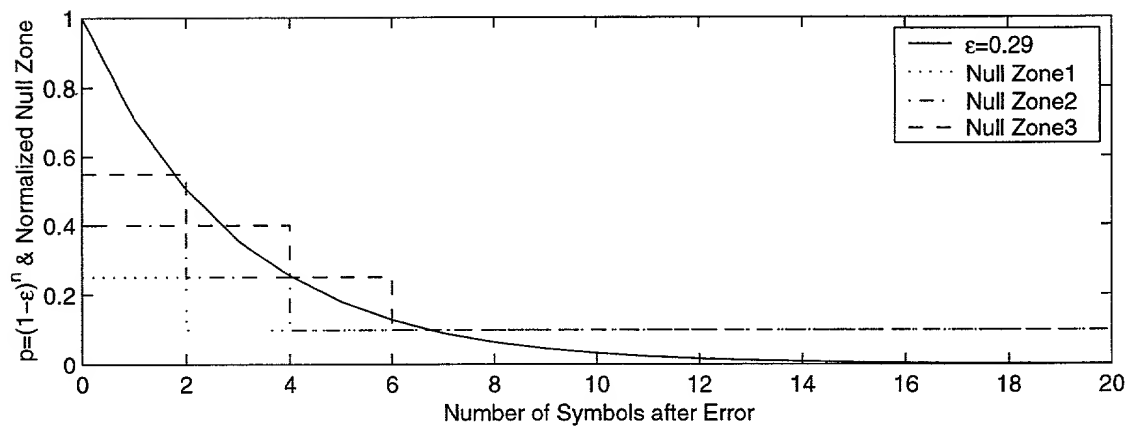


FIG. 7

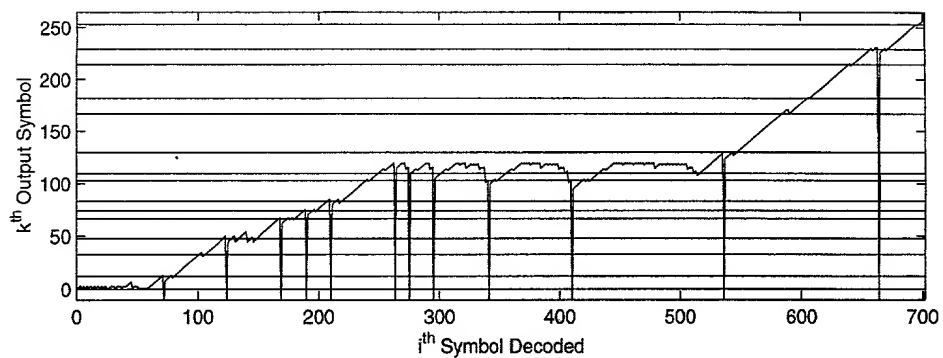


FIG. 8a

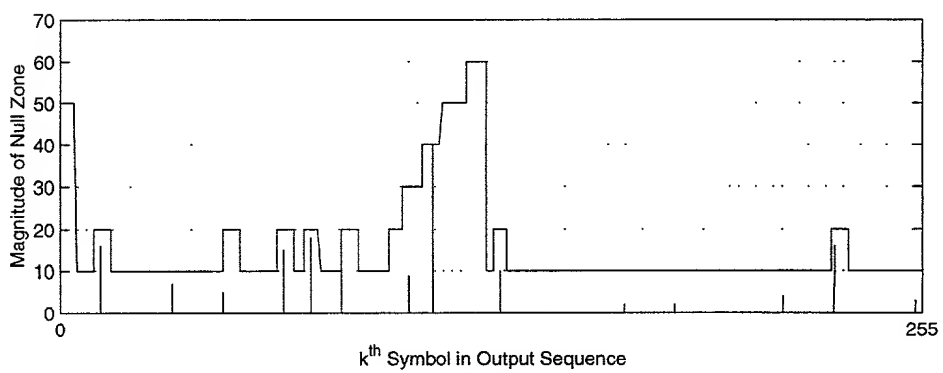


FIG. 8b

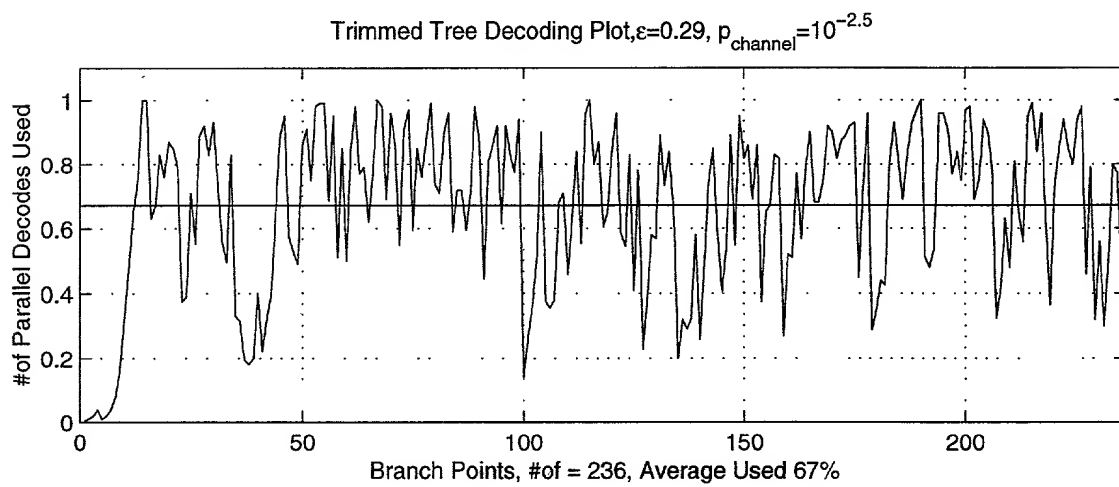


FIG. 9

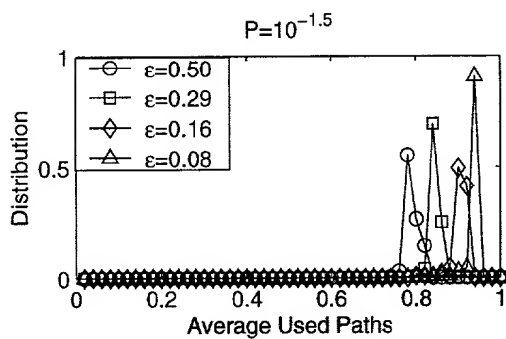


FIG. 10a

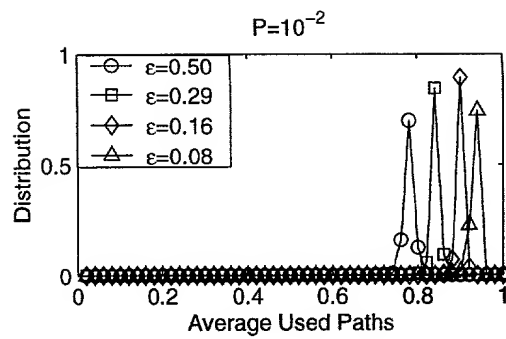


FIG. 10b

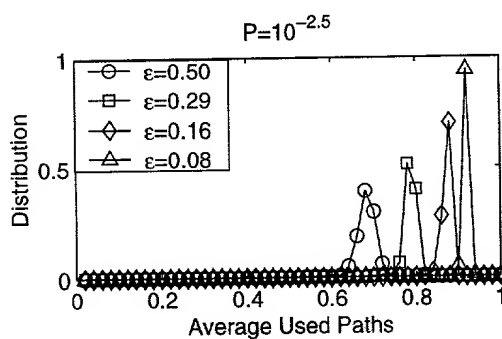


FIG. 10c

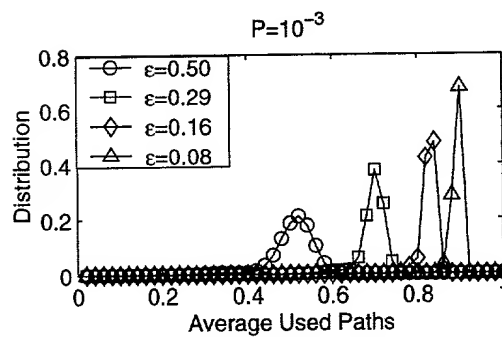


FIG. 10d

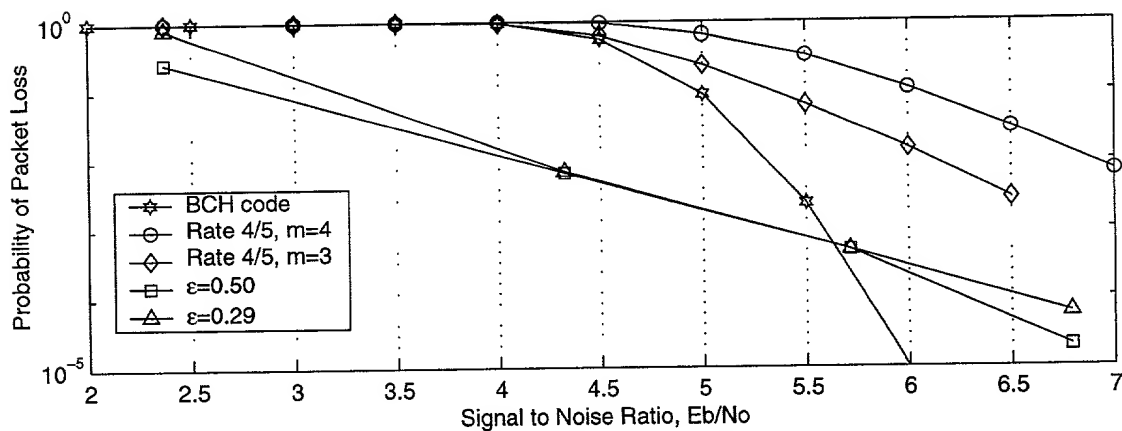


FIG. 11